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(54) Phase-locked loop system with compensation for data-transition-dependent variations in loop gain

Phasenregelkreissystem mit Kompensierung der Änderungen der datenflankenabhängigen Schleifenverstärkung

Système de boucle à verrouillage de phase comportant une compensation de la variation du gain de boucle en fonction des transitions des données

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Description

Background of the Invention

[0001] This invention relates to phase locked loop (PLL) systems in which the density of data transitions in the data signal varies.

[0002] Monolithic PLL circuits have become the basic building blocks of many consumer and industrial electronic systems. In telecommunication data systems, for example, the PLL is an integral part of the clock recovery subsystem. The PLL may be used to recover the clock signal from the data signal; the recovered clock may then be used, for example, to regenerate the data signal.

[0003] The basic PLL system generally comprises three elements: (1) a phase detector, (2) a loop filter, and (3) a voltage controlled oscillator (VCO), which are interconnected in a feedback system as shown in FIG. 12.1 of "Bipolar and MOS Analog Integrated Circuit Design," A. B. Grebene, John Wiley & Sons (1984). The phase detector compares the phase of an input signal V_s with the phase of the VCO and generates a control voltage V_d. This voltage V_d is filtered by the loop filter, the output of which is applied to the control terminal of the VCO to control its frequency of oscillation.

[0004] The loop gain, K_L, of the PLL is defined as follows:

$$K_L = K_D K_o \quad (1)$$

where K_D (V/rad) is the phase detector conversion gain, and K_o (HZ/V) is the voltage-to-frequency conversion gain of the VCO.

[0005] It is well known that the phase detector gain K_D, and hence the loop gain, of a clock recovery PLL is dependent on the transition density of the data signal. (D.L. Duttweiler, BSTJ, Vol. 55, No. 1 (1976)). That is, when the data signal undergoes few data transitions, the phase detector has periods of time when no data transitions occur to compare with the VCO recovered clock. The effective phase detector gain K_{DD} is then degraded by a factor $D < 1$ defined as

$$D = f_{trans} / f_{clk} \quad (2)$$

and

$$K_{DD} = K_D D \quad (3)$$

where f_{trans} is the frequency of the data transitions and f_{clk} is the frequency of the recovered clock.

[0006] Consider two cases illustrated by FIGS. 1 and 2. In both cases the PLL is locked to an input data signal, but the clock signal is lagging the data signal by a phase error Δ. In FIG. 1, there is only one rising clock cycle transition between adjacent data transitions; thus, the degrading factor D = 1. But, in FIG. 2, there are three rising clock cycle transitions between adjacent data transitions; thus D = 1/3. Therefore, there are three times the number of error corrections in the D = 1 case than in the D = 1/3 case. This difference effectively makes the phase detector gain of FIG. 2, $K_{D2} = 1/3\, K_{D1}$, where K_{D1} is the phase detector gain of FIG. 1, even though the phase detectors themselves have physically the same implementation.

[0007] This data-dependent variation of the phase detector gain will cause variations in the PLL closed loop dynamics and may be undesirable. For example, in a second order active loop filter PLL (Grebene, supra, FIG. 12.9), the natural frequency, the damping factor and the 3dB frequency all decrease as K_{DD} decreases, but the jitter peaking increases. This effect is particularly troublesome in systems in which the PLLs (or repeaters which include the PLLs) are cascaded. For example, in token ring systems data may be inserted/extracted at different nodes such that different repeaters/PLLs see different data streams. With prior art PLLs, the transfer function of the PLL shifts with transition density such that some PLLs may lose lock; others may not.

[0008] FR-A-2,662,875 describes a tuning circuit with a phase control loop and a frequency control loop, characterized in that, for comparison by an integrator, the current progressively increases with the closing time or the phase error of the corresponding branch of a phase discriminator.

Summary of the Invention

[0009] The invention is as set out in the claims.

[0010] The loop gain of a PLL is made to be essentially constant by compensating for the dependence of that gain on the data transition density of an input data signal. The loop gain is made to be controllably responsive to the transition density of the input data signal so as to increase the loop gain when the density is relatively low and, conversely, to decrease the gain when the density is relatively high. In one embodiment of this method, the number of clock transitions (either rising or falling) between adjacent data transitions is counted and used to adjust the loop gain. In a preferred embodiment, the average loop gain is essentially constant with changes in transition density.

[0011] This method is illustratively implemented in a PLL which includes a modulator for altering the loop gain in response to the difference between the data transition density of the input signal and the clock signal. Illustratively the modulator comprises a charge pump located between the phase detector and the loop filter. The charge pump supplies current pulses to the filter, the amplitude of the pulses being related to the data transition density; the lower the data transition density in a given time interval, the higher the pulse amplitude (and

conversely).

[0012] The invention is particularly attractive for use in systems in which there is an upper bound on the number of data bits which can occur without a data transition also occurring. Examples of such systems are those employing Manchester coding or Run Length Limited coding schemes.

[0013] It is also attractive for use in systems where the PLLs are cascaded because the PLL transfer functions, like the loop gain, are independent of transition density and, so, regardless of what data stream a PLL sees, it always maintains the locked condition.

Brief Description of the Drawings

[0014] The invention, together with its various features and advantages, can be readily understood from the following more detailed description taken in conjunction with accompanying drawing, in which:

FIGS. 1 and 2 are waveforms used to describe the adverse effect of data transition dependent gain on PLL performance;

FIG. 3 is a block diagram of a PLL system in accordance with one embodiment of the invention;

FIG. 4 is a combined block diagram and circuit schematic of the embodiment of FIG. 3;

FIG. 5 shows waveforms useful in explaining the operation of the embodiment of FIG. 4; and

FIG. 6 is an illustrative implementation of the counter of FIG. 3.

Detailed Description

[0015] As noted above, the invention in general makes the loop gain of a PLL system controllably responsive to the transition density of a data signal. In particular, the invention makes the loop gain essentially constant even though the transition density may vary.

[0016] A block diagram of a PLL system 10 in accordance with one embodiment of the invention is shown in FIG. 3. The system includes a feedback loop 12 formed by a phase detector 14, a loop gain modulator (e.g., a charge pump 16), a loop filter 18, and a voltage controlled oscillator (VCO) 20. Located outside the loop 12, a data transition comparator 22 compares the transitions of the input data signal V_s with those of the clock V_o (i.e., the VCO output) and generates pulse width modulated (PWM) control pulses V_T. The PWM pulses V_T control the magnitude of pulse amplitude modulated (PAM) current pulses I_c supplied by charge pump 16 to loop filter 18. The latter, in turn, generates a control voltage V_c which controls the frequency of VCO 20. Loop filter 18, which may be active or passive, VCO 20, which may be a relaxation oscillator, and transition comparator 22, which may simply be a differentiator followed by rectifier, are all well-known in the art.

[0017] Phase detector 14 may be any one of a class of well known detectors suitable for handling non-periodic data signals. As shown in FIG. 3, phase detector 14 has two inputs: the input data signal V_s and the output signal (clock) V_o of VCO 20. Detector 14 compares the phases of V_s and V_o and generates two outputs, V_d and V_u, but three allowable states. That is, these outputs are logic levels applied to the charge pump 16: (1) V_u alone is true when the output frequency of VCO 20 needs to be increased, (2) V_d alone is true when the output frequency of VCO 20 needs to be decreased, and (3) V_u and V_d are false simultaneously when the output frequency of VCO 20 is to remain unchanged. Both V_d and V_u are never true simultaneously. This type of tri-state phase detector used in conjunction with a charge pump is described by F. M. Gardner in an article entitled "Charge-Pump Phase-Lock Loops," IEEE Transactions on Communications, Vol. COM-28, No. 11, p. 1849 (1980). Although Gardner describes the charge pump as "nothing but a three-position, electronic switch that is controlled by the three states" of the phase detector, in our PLL the combination of the charge pump 16 and the data transition comparator 22 function in a unique manner to supply PAM current pulses I_c to the loop filter 18. The amplitude of these pulses is related to the transition density of the input data signal V_s. Since the transition density changes as a function of time, the PLL dynamically adjusts the current pulse amplitudes so that the phase detector gain, and hence the loop gain, compensates for variations in density. Effectively, therefore, the gain and hence the loop dynamics are maintained essentially constant over a relatively wide range of data transition densities.

[0018] The effective phase detector gain (and hence the loop gain) is dynamically adjusted by means of charge pump 16 and comparator 22. The comparator 22 counts the number of clock cycles n which occur between data transitions and generates a suitable control signal V_T which enables the charge pump 16 to deliver a current pulse of amplitude nI to the loop filter 18. For example, in FIG. 2 (the case of a degrading factor of D = 1/3) during the interval $t_o - t_1$, three clock cycles have occurred before the data transition at t_1. Consequently, the comparator 22 supplies a suitable control signal V_T to charge pump 16 so that a current pulse of amplitude 3I (not shown in FIG. 2) is applied to the loop filter at approximately t_1. The sign of the pulse may be either positive or negative depending on whether the clock signal is lagging or leading the data signal, respectively.

[0019] The manner in which the PAM control current is generated can be better understood from the following more detailed description of FIGS. 4-6 in which corresponding components of FIG. 3 and FIG. 4 have been given identical reference numerals. In this embodiment the loop filter 18 is a standard second-order filter having the series combination of a resistor R_1 and a capacitor C_1 connected between its input terminal and ground, with smoothing capacitor C_2 connected in parallel with the R_1-C_1 combination. On the other hand, the data tran-

sition comparator 22 comprises a data transition detector 22.1 (e.g., a differentiator followed by a rectifier) with its input coupled to V_s and its output coupled to the clear input CLR of counter 22.2. The increment input INC of the counter is coupled to V_o, whereas the parallel outputs of the counter are control voltages V_{Ti} (i = 2, 3, 4...) coupled to the charge pump 16 so as to control the state of switches S_i and S'_i (i=2, 3, 4 ...).

[0020] The charge pump itself includes a first bank 16.1 of parallel - connected current sources I_i (i = 1, 2, 3...) coupled through switch S1 to node N for delivering a positive current control pulse I_c of amplitude nI (n=1, 2, 3...) to the loop filter, and, similarly, a second bank 16.2 of parallel-connected current sources I'_i (i = 1, 2, 3...) coupled through switch S1' to node N for delivering a negative current control pulse I_c to the loop filter. The amplitude of the current pulses is determined by the number of switches S_i or S'_i (i = 2, 3, 4...) which are closed under control of V_{Ti}, whereas the duration (width) of the current pulse I_c is determined the length of time that switches S1 or S1' are closed under control of the phase detector outputs V_u and V_d, respectively. Thus, the width of the current pulses I_c is related to the phase error generated by the phase detector and as a result may vary considerably (e.g., 0-50%). In the interest of simplicity, however, FIG. 5 shows the pulses I_c to be of equal duration.

[0021] In operation of the embodiment of FIG. 4, the phase detector 14 compares the rising edge (for example) of the clock signal V_o to a data transition of input signal V_s. Assuming a positive VCO gain K_o and an "early" clock transition, then a pulse would be generated on the "down" output V_d. This pulse would cause the control voltage V_c to decrease, thus slowing the frequency of V_o (i.e., the clock rate). Note, however, the clock in FIG. 5 is shown to have a constant frequency in the interests of simplicity (i.e., in many cases the actual frequency shift would be imperceptible in a schematic drawing). Conversely, if the clock transition were "late", a pulse would be generated on the "up" output V_u to accelerate the clock rate.

[0022] Consider now the operation of charge pump 16 in which we assume each current source supplies a current of magnitude I. A pulse on V_u closes switch S1 and connects bank 16.1 to loop filter 18. The amplitude of the control current I_c supplied to the filter is I + kI; that is I (from I_1) plus kI (k = 0, 1, 2...) depending on how many of the switches S_i (i = 2, 3...) are closed. The duration of I_c is dependent on the duration of V_u. Similar comments apply to a pulse V_d applied to switch S1'. In both cases counter 22.2 controls the closure of switches S_i and S'_i (i = 2, 3...) by counting the number of clock transitions which occur between adjacent data transitions. If a data transition occurs (t_o, FIG. 5), transition detector 22.1 clears the counter 22.2 and V_{Ti} (i = 2, 3...) are all set to zero, thus disabling the current sources I_i and I'_i (i = 2, 3...). If a data transition occurs after t_o, the current source I_i or I'_i supplies the necessary control current. However, if no data transition occurs by the second rising clock edge at t_1, as shown in FIG. 5, then V_{T2} goes high on the trailing edge of that clock cycle (at t_2) which closes switches S_2 and S'_2 and prepares I_2 and I'_2 for injection of control current into the loop filter. (As noted earlier, whether the positive control current I_2 or the negative one I'_2 is injected depends on whether a pulse appears on V_u or V_d.) Similarly, if there continues to be no data transition by t_3, the rising edge of the third clock cycle, then at t_4 V_{T3} goes high, closes S_3 and S'_3 so that current sources I_3 and I'_3 are prepared to inject current into the loop filter. Note, during the interval t_o - t_5 when there is no data transition, both V_u and V_d are low, the third state of the tri-state phase detector. Finally, when a data transition occurs at t_5, the phase detector detects the transition and applies a control voltage V_d to the charge pump so that a control current pulse I_c = -3I is applied to the loop filter. In a similar fashion, FIG. 5 shows, for example, additional control current pulses of amplitude +2I, -I, +4I, -I, -I, and +I, respectively, being generated by the charge pump at times t_6 to t_{11}, respectively. In this manner, the phase detector gain, and hence the loop gain, is adjusted to compensate for the changing transition density of the data signal.

[0023] It is to be understood that the above-described arrangements are merely illustrative of the many possible specific embodiments which can be devised. For example, there are many alternative designs of counter 22.2 well-known in the art which would be suitable for use in the inventive PLL system. One such design is shown in FIG. 6 wherein a plurality of D-flip flops are arranged in tandem. A dc voltage corresponding to a logic state is applied to the D input of the first flip flop, and the control voltages (V_{Ti}) (i = 2, 3...) are taken from the Q outputs of the respective flip flops. The increment signal INC from the VCO is applied to the clock inputs CLK of the flip flops, and the clear signal CLR from the data transition detector 22.1 is applied to their clear inputs.

[0024] In addition, although the foregoing description relates, for illustrative purposes, to analog PLL systems, the principles of the invention are also applicable to all-digital PLLs, e.g., a PLL with a digital loop filter and digital phase detector, a PLL implemented in an FPGA or a DSP, or a PLL implemented in software in a microprocessor.

[0025] Finally, it should be noted that the invention is advantageously used in systems where the data is coded so that there is an upper bound on the number of data bits which can occur between data transitions. Examples of such coding schemes are Manchester coding and Run Length Limited coding. However, the invention is not limited to such use in such systems. Thus, if the embodiments of the invention shown in FIG. 3 or FIG. 4 were used in system without an upper bound of the type described above, then the PLL would still provide loop gain compensation, and hence be an improvement over the prior art, up to the point where the charge pump

had already switched in the maximum number of current sources provided by the physical design even though a relatively low transition density data signal may be "demanding" more current.

Claims

1. A method of operation of a phase-locked loop system for locking a clock signal to an input data signal, a method characterized by the steps of:

   (a) determining the transition density of the input data signal by counting the number of clock signal transitions which occur between data signal transitions, and
   (b) adjusting the loop gain of said system in response to said counting step (a).

2. The method of claim 1 wherein, in step (b) the average loop gain is maintained essentially constant with changes in transition density of the input signal.

3. The method of claim 1 wherein said system includes a phase detector for comparing the phase of said input signal to that of said clock signal and wherein step (b) includes adjusting the effective gain of said phase detector, in response to said counting step (a).

4. The method of claim 3 wherein said system includes a loop filter for filtering the output of said phase detector and wherein step (b) includes injecting current pulses into said loop filter, the amplitude of said pulses being related to the number of said transitions counted in step (a).

5. The method of claim 4 wherein said injecting step includes using the output of said phase detector to determine when said current pulses are injected into said loop filter.

6. The method of claim 4 wherein the amplitude of said pulses is related to said number of clock transitions, wherein said data and clock signals are out of phase by an amount Δ, and wherein the width of said pulses is related to Δ.

7. A data system (10) comprising
   a phase-locked loop subsystem (12) for locking a clock signal (V_o) an input data signal (V_s), said loop subsystem having a characteristic loop gain related to the difference Δ in phase between said input signal and said clock signal, and characterized by a modulator (16,22) for adjusting said loop gain in response to the difference between the data transition density of said input signal and that of said clock signal.

8. The system of claim 7 wherein said modulator (16,22) adjusts the loop gain in a manner to maintain the average loop gain essentially constant with changes in the density of said input signal.

9. The system of claim 7 wherein said modulator includes

   a comparator (22) for generating a first control signal related to said difference in data transition density, and
   a source (16) for injecting current pulses into said loop in response to said first control signal.

10. The system of claim 9 wherein

    said comparator (22) counts the number of rising (or falling) clock signal transitions between adjacent data signal transitions, and
    said source (16) injects pulses the amplitudes of which are related to said numbers counted by said comparator.

11. The system of claim 10 wherein

    said loop subsystem (12) includes a tri-state phase detector (14) for generating second control signals responsive to the difference in phase between said input signal and said clock signal, and
    the timing of the injection of said pulses is responsive to said second control signals generated by said phase detector.

12. The system of claim 11 wherein
    said loop subsystem comprises an oscillator (20) for generating said clock signal, a loop filter (18) for providing a filtered third control signal (V_c) for adjusting the frequency of said oscillator, and said source (16) supplies said current pulses to said filter so as to generate said third control signal.

13. The system of claim 7 wherein said modulator includes a charge pump (16) which injects current pulses into said loop, wherein the magnitude of said pulses is related to the number of clock transitions which occur between data transitions, and wherein the width of said pulses is related to Δ.

Patentansprüche

1. Verfahren zum Betreiben eines Phasenregelkreissystems zum Einrasten eines Taktsignals auf ein Eingangsdatensignal,
   gekennzeichnet durch die Verfahrensschritte:

   a) Ermitteln der Übergangsdichte des Ein-

gangsdatensignals durch Zählen der Anzahl der Taktsignalübergänge, die zwischen den Datensignalübergängen auftreten, und
b) Einstellen der Schleifenverstärkung des Systems unter Ansprechen auf den Zählschritt a).

2. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß in Schritt b) die mittlere Schleifenverstärkung bei Änderungen der Übergangsdichte des Eingangssignals im wesentlichen konstant gehalten wird.

3. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß das System einen Phasendetektor zum Vergleichen der Phase des Eingangssignals mit der des Taktsignals umfaßt und daß Schritt b) das Einstellen der effektiven Verstärkung des Phasendetektors unter Ansprechen auf den Zählschritt a) umfaßt.

4. Verfahren nach Anspruch 3, dadurch gekennzeichnet, daß das System ein Schleifenfilter zum Filtern des Ausgangssignals des Phasendetektors umfaßt und daß Schritt b) das Einspeisen von Stromimpulsen in das Schleifenfilter umfaßt, wobei die Impulsamplituden sich auf die Anzahl der Übergänge, die in Schritt a) gezählt worden sind, beziehen.

5. Verfahren nach Anspruch 4, dadurch gekennzeichnet, daß der Einspeiseschritt das Verwenden des Ausgangssignals des Phasendetektors umfaßt, um zu bestimmen, wann die Stromimpulse in das Schleifenfilter eingespeist werden.

6. Verfahren nach Anspruch 4, dadurch gekennzeichnet, daß sich die Amplitude der Impulse auf die Anzahl der Taktübergänge bezieht, und daß das Daten- und das Taktsignal einen Phasenunterschied des Betrags Δ aufweisen, und daß sich die Impulsbreite auf Δ bezieht.

7. Datensystem (10), umfassend:
ein Phasenregelkreis-Untersystem (12) zum Einrasten eines Taktsignals (V_o) auf ein Eingangsdatensignal (V_s), wobei das Schleifen-Untersystem eine charakteristische Schleifenverstärkung aufweist, die sich auf die Phasendifferenz Δ zwischen dem Eingangssignal und dem Taktsignal bezieht, gekennzeichnet durch:
einen Modulator (16, 22) zum Einstellen der Schleifenverstärkung unter Ansprechen auf die Differenz zwischen der Datenübergangsdichte des Eingangssignals und der des Taktsignals.

8. System nach Anspruch 7, dadurch gekennzeichnet, daß der Modulator (16, 22) die Schleifenverstärkung derart einstellt, daß die mittlere Schleifenverstärkung bei Änderungen der Dichte des Eingangssignals im wesentlichen konstant bleibt.

9. System nach Anspruch 7, dadurch gekennzeichnet, daß der Modulator umfaßt:
einen Komparator (22) zum Erzeugen eines ersten Steuersignals, das mit der Differenz der Datenübergangsdichte in Beziehung steht, und eine Quelle (16) zum Einspeisen von Stromimpulsen in die Schleife als Reaktion auf das erste Steuersignal.

10. System nach Anspruch 9, dadurch gekennzeichnet,
daß der Komparator (22) die Anzahl der ansteigenden (oder abfallenden) Taktsignalübergänge benachbarter Datensignalübergänge zählt, und daß
die Quelle (16) Impulse einspeist, deren Amplituden in Beziehung zu der vom Komparator gezählten Anzahl stehen.

11. System nach Anspruch 10, dadurch gekennzeichnet, daß
das Schleifen-Untersystem (12) einen Tri-State-Phasendetektor (14) zum Erzeugen eines zweiten Steuersignals unter Ansprechen auf die Phasendifferenz zwischen dem Eingangssignal und dem Taktsignal enthält, und daß
die Zeitsteuerung des Einspeisens der Impulse eine Reaktion auf das vom Phasendetektor erzeugte zweite Steuersignal ist.

12. System nach Anspruch 11, dadurch gekennzeichnet, daß das Schleifen-Untersystem einen Oszillator (20) zum Erzeugen des Taktsignals und ein Schleifenfilter (18) zum Bereitstellen eines gefilterten dritten Steuersignals (V_c) zum Einstellen der Frequenz des Oszillators umfaßt, und daß die Quelle (16) Stromimpulse an das Filter zum Erzeugen des dritten Steuersignals anlegt.

13. System nach Anspruch 7, dadurch gekennzeichnet, daß der Modulator eine Ladungspumpe (16) umfaßt, die Stromimpulse in die Schleife einspeist, daß die Impulsamplitude in Beziehung zur Anzahl der Taktübergänge steht, die zwischen den Datenübergängen auftreten, und daß die Impulsbreite in Beziehung zu Δ steht.

Revendications

1. Procédé de mise en fonctionnement d'un système de boucle à verrouillage de phase destiné à verrouiller un signal d'horloge sur un signal de données d'entrée, ce procédé étant caractérisé par les étapes :

   (a) de détermination de la densité de transitions du signal de données d'entrée en comptant le nombre de transitions du signal d'horloge qui apparaissent entre des transitions du signal de données, et
   (b) d'ajustement du gain de boucle du système en réponse à l'étape de comptage (a).

2. Procédé suivant la revendication 1, dans lequel, lors de l'étape (b), le gain de boucle moyen est maintenu pratiquement constant lors de variations de la densité de transitions du signal d'entrée.

3. Procédé suivant la revendication 1, dans lequel le système comporte un détecteur de phase destiné à comparer la phase du signal d'entrée à celle du signal d'horloge et dans lequel l'étape (b) comprend l'ajustement du gain effectif du détecteur de phase en réponse à l'étape de comptage (a).

4. Procédé suivant la revendication 3, dans lequel le système comporte un filtre de boucle destiné à filtrer la sortie du détecteur de phase et dans lequel l'étape (b) comprend l'injection d'impulsions de courant dans le filtre de boucle, l'amplitude des impulsions étant liée au nombre de transitions comptées lors de l'étape (a).

5. Procédé suivant la revendication 4, dans lequel l'étape d'injection comprend l'utilisation de la sortie du détecteur de phase pour déterminer l'instant où les impulsions sont injectées dans le filtre de boucle.

6. Procédé suivant la revendication 4, dans lequel l'amplitude des impulsions est liée au nombre de transitions d'horloge, dans lequel les données et les signaux d'horloge sont déphasés d'une quantité Δ, et dans lequel la largeur des impulsions est liée à Δ.

7. Système de données (10) comprenant :
   un sous-système (12) de boucle à verrouillage de phase pour verrouiller un signal d'horloge (V_o) sur un signal de données d'entrée (V_s), le sous-système de boucle ayant un gain de boucle caractéristique lié à la différence Δ de phase entre le signal d'entrée et le signal d'horloge, et caractérisé par un modulateur (16, 22) destiné à ajuster le gain de boucle en réponse à la différence entre la densité de transitions de données du signal d'entrée et celle du signal d'horloge.

8. Système suivant la revendication 7, dans lequel le modulateur (16, 22) ajuste le gain de boucle de manière à maintenir pratiquement constant le gain de boucle moyen lors de variations de la densité du signal d'entrée.

9. Système suivant la revendication 7, dans lequel le modulateur comporte :

   un comparateur (22) destiné à générer un premier signal de commande lié à la différence de densité de transitions de données, et
   une source (16) destinée à injecter des impulsions de courant dans la boucle en réponse au premier signal de commande.

10. Système suivant la revendication 9, dans lequel

    le comparateur (22) compte le nombre de transitions de signal d'horloge montantes (ou descendantes) entre des transitions adjacentes du signal de données, et
    la source (16) injecte des impulsions dont les amplitudes sont liées aux nombres comptés par le comparateur.

11. Système suivant la revendication 10, dans lequel

    le sous-système (12) de boucle comporte un détecteur (14) de phase à trois états destiné à générer des seconds signaux de commande en réponse à la différence de phase entre le signal d'entrée et le signal d'horloge, et
    le cadencement de l'injection des impulsions est sensible aux seconds signaux de commande générés par le détecteur de phase.

12. Système suivant la revendication 11, dans lequel :
    le sous-système de boucle comprend un oscillateur (20) destiné à générer le signal d'horloge, un filtre (18) de boucle destiné à fournir un troisième signal (V_c) de commande pour ajuster la fréquence de l'oscillateur, et la source (16) délivre les impulsions de courant au filtre afin de générer le troisième signal de commande.

13. Système suivant la revendication 7, dans lequel le modulateur comporte une pompe (16) de charge qui injecte des impulsions de courant dans la boucle, dans lequel le niveau des impulsions est lié au nombre de transitions d'horloge qui apparaissent entre des transitions de données, et dans lequel la largeur des impulsions est liée à Δ.

FIG. 1

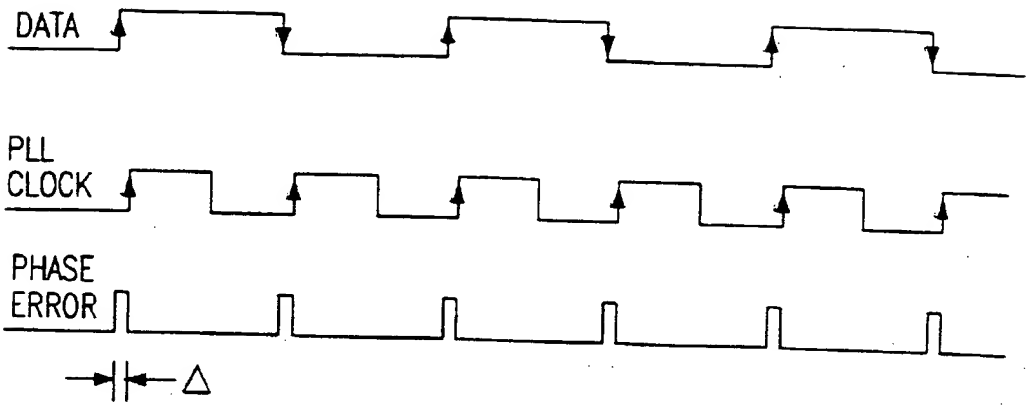

DATA
PLL
CLOCK
PHASE
ERROR
Δ

FIG. 2

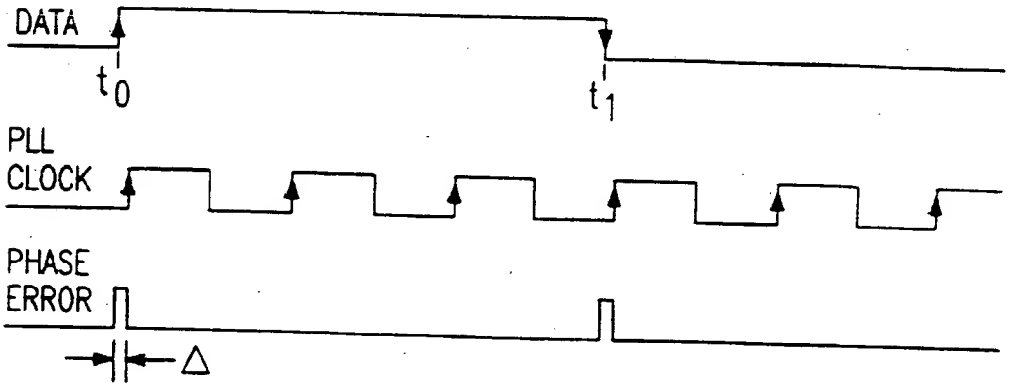

DATA
t0
t1
PLL
CLOCK
PHASE
ERROR
Δ

FIG. 3

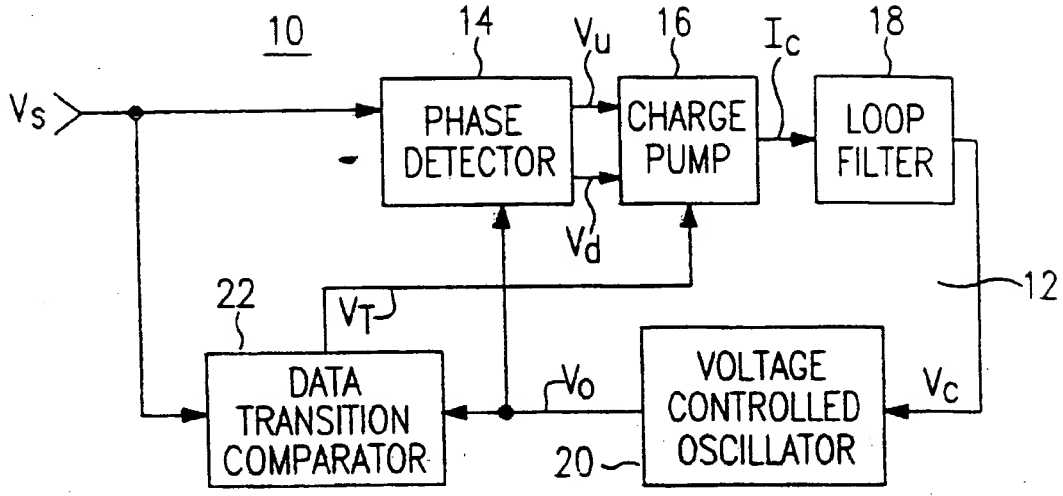
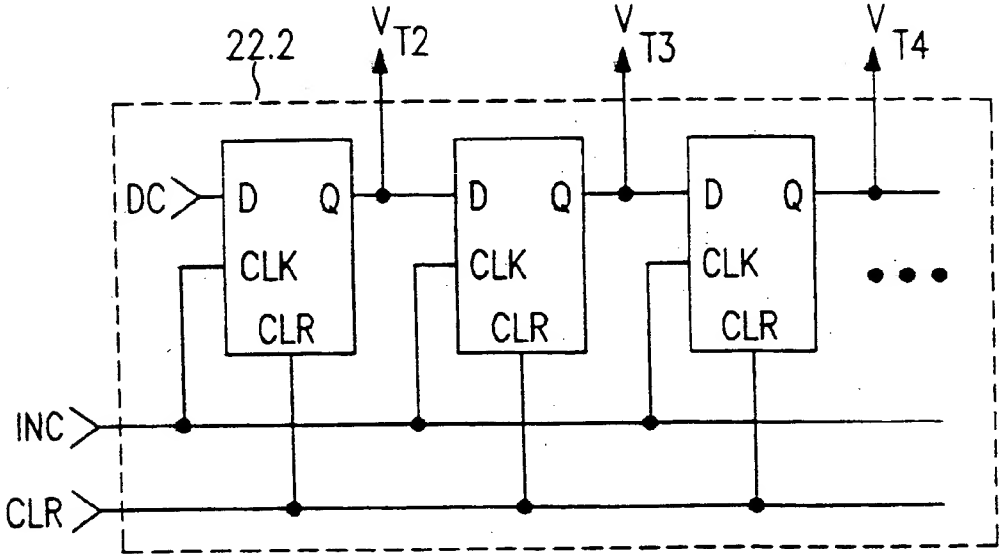

10
14
V_u
16
I_c
18
V_s
PHASE DETECTOR
CHARGE PUMP
LOOP FILTER
V_d
12
22
V_T
DATA TRANSITION COMPARATOR
V_o
VOLTAGE CONTROLLED OSCILLATOR
V_c
20

FIG. 6


22.2
V_{T2}
V_{T3}
V_{T4}
DC
D
Q
CLK
CLR
INC
CLR

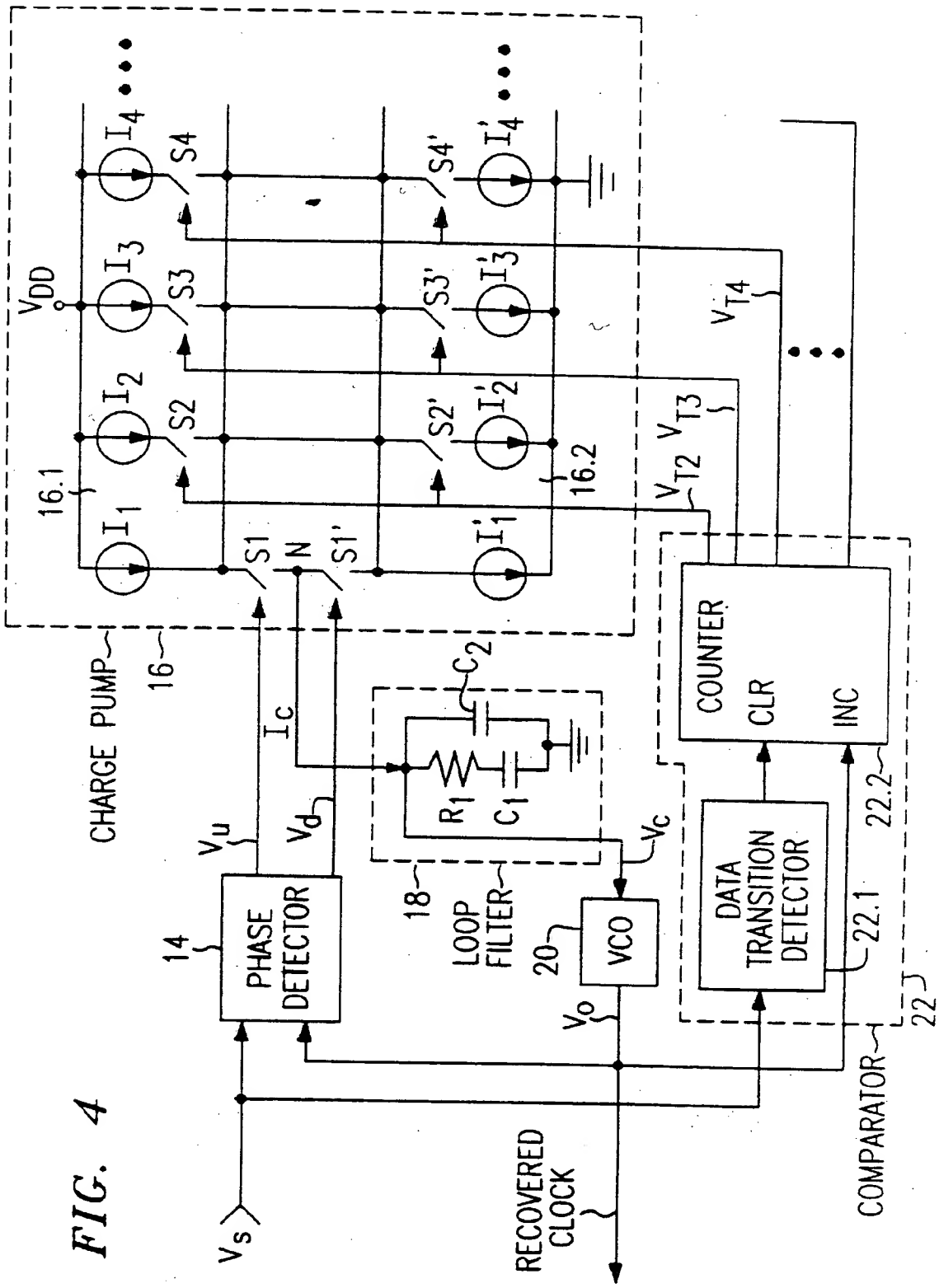
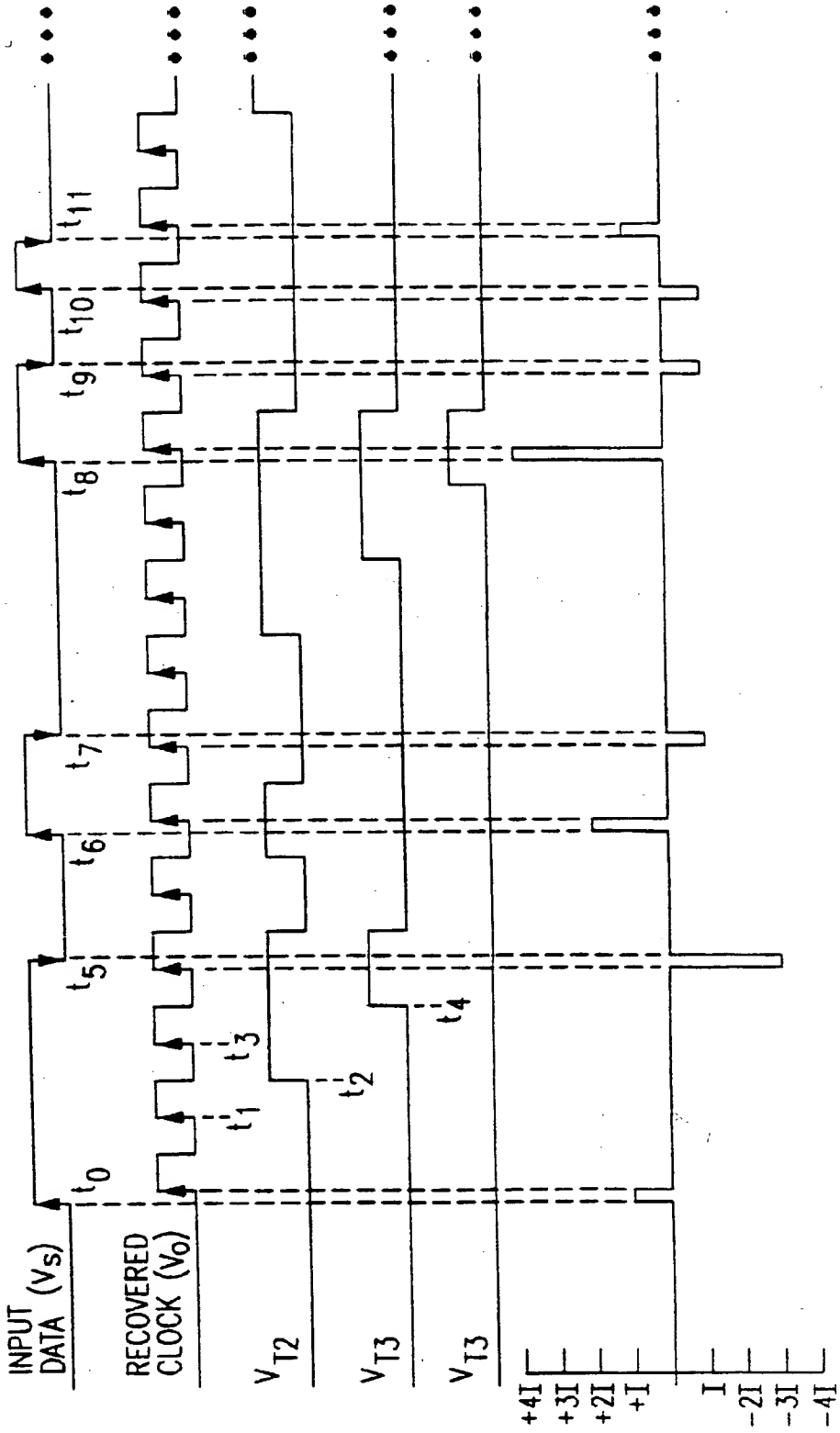

V_{DD}
I_1
I_2
I_3
I_4
I'_1
I'_2
I'_3
I'_4
S1
S2
S3
S4
S1'
S2'
S3'
S4'
N
16.1
16.2
V_{T2}
V_{T3}
V_{T4}
CHARGE PUMP
16
I_C
C_2
R_1
C_1
18
LOOP FILTER
V_u
V_d
V_c
14
PHASE DETECTOR
20
VCO
V_o
V_s
RECOVERED CLOCK
COUNTER
CLR
INC
DATA TRANSITION DETECTOR
22.1
22.2
22
COMPARATOR

FIG. 4

FIG. 5


INPUT DATA (V_S)
RECOVERED CLOCK (V_O)
V_{T2}
V_{T3}
V_{T3}
t_0
t_1
t_2
t_3
t_4
t_5
t_6
t_7
t_8
t_9
t_{10}
t_{11}
+4I
+3I
+2I
+I
I
-2I
-3I
-4I